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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/803,203	Confirmation No.:	5841
First Named Inventor:	Bulucea, Constantin	Filing Date:	17 March 2004
Group Art Unit:	2811	Examiner:	Unknown
Atty. Docket No.:	NS-5737 US		
Title:	Configuration and Fabrication of Semiconductor Structure Having N-channel Channel-junction Field-effect Transistor		
Assignee(s):	National Semiconductor Corporation		

Mountain View, California
23 September 2004

COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.97(b)

Sir:

Pursuant to 37 CFR 1.56, 1.97, and 1.98, each document listed on the accompanying substitute PTO Form 1449 is called to the attention of the Examiner for the above patent application. A copy of each listed document is enclosed.

Nishiuchi et al., Hu et al., and the first-listed Other Art document of Parillo et al. cited here respectively are Nishiuchi et al., Hu et al., and Parillo et al. cited on pages 4 and 5 of the specification of the present application subject to the publication-date information being made more specific for these three documents in the accompanying substitute PTO Form 1449.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

Nishida et al. cited here is Nishida et al. cited on page 5 of the specification of the present application subject to the publication-source information being corrected from IRPS Dig. Tech. Paps. as given in the specification to IEDM Tech. Dig. as specified in the accompanying substitute PTO Form 1449. The publication-date information for Nishida et al. has also been made more specific in the substitute PTO Form 1449.

In contrast to U.S. Patent 6,548,842 B1 in which both the n-channel and p-channel insulated-gate field-effect transistors ("IGFETs") of a complementary-IGFET structure are surface-channel devices, Nakahara et al. proposes a complementary-IGFET structure in which both the n-channel and p-channel IGFETs are channel-junction (buried-channel) devices.

Citation of each listed document shall not be construed as:

1. an admission that the document is necessarily prior art with respect to the instant invention;

2. a representation that a search has been made; or

3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b).

This information disclosure statement is submitted under the provisions of 37 CFR 1.97(b).

EXPRESS MAIL LABEL NO.:

EV 337 116 005 US

Respectfully submitted,

Ronald J. Meetin

Ronald J. Meetin
Attorney for Applicant(s)
Reg. No. 29,089

210 Central Avenue
Mountain View, CA 94043-4869

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

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Substitute PTO Form 1449	Bulucea, Constantin	5841
	Filing Date	Group
	17 March 2004	2811

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,047,358	09/1991	Kosiak et al.	437	034	
	AB	5,672,521	09/1997	Barsan et al.	437	024	
	AC	5,942,780	08/1999	Barsan et al.	257	321	
	AD	5,952,701	09/1999	Bulucea et al.	257	407	
	AE	6,051,482	04/2000	Yang	438	526	
	AF	6,194,293 B1	02/2001	Krivokapic	438	525	
	AG	6,548,842 B1	04/2003	Bulucea et al.	257	288	
	AH	6,576,966 B1	06/2003	Bulucea	257	408	
	AI						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AJ	298,421 A2	05/1988	Europe	027	010		
	AK							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AL	Appels et al., "Local Oxidation of Silicon and Its Applications in Semiconductor-Device Technology", Philips Res. Rpts., vol. 25, 1970, pp. 118 - 132
	AM	Black et al., "CMOS Process for High-performance Analog LSI", IEDM Tech. Dig., 1976, pp. 331 - 334
	AN	Bohr, "Industry-Leading Transistor Performance Demonstrated on Intel's 90-nanometer Logic Process", Intel Corp., ftp://download.intel.com/research/ silicon/90nm_press_briefing-technical.pdf, 13 Aug. 2002, pp. 1 - 21
	AO	Bohr, "Intel's 90 nm Logic Technology Using Strained Silicon Transistors", Intel Corp., www.intel.com/research/downloads/Bohr-Strained-Silicon-120403.pdf, Dec. 2003, pp. 1 - 10
	AP	Brederlow et al., "Hot Carrier Degradation of the Low Frequency Noise of MOS Transistors under Analog Operating Conditions", 37th Ann. IEEE Int'l Rel. Phys. Symp. Procs., 23 - 25 Mar. 1999, pp. 239 - 242
	AQ	Brown, "Trends in Advanced Process Technology-Submicrometer CMOS Device Design and Process Requirements", Procs. IEEE, Dec. 1986, pp. 1678 - 1702
	AR	Bulucea et al., "Threshold Voltage Control in Buried-Channel MOSFETs", Solid-State Electronics, vol. 41, no. 9, 1997, pp. 1345 - 1354
	AS	Chaparala et al., "NBTI in Dual Gate Oxide PMOSFETs", 2003 8th Int'l Symp. on Plasma- and Process-Induced Damage, 24 and 25 Apr. 2003, pp. 138 - 141

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

EXPRESS MAIL LABEL NO.: EV 337 116 005 US

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Substitute PTO Form 1449	Bulucea, Constantin	Unknown
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
	BA	Chen, CMOS Devices and Technology for VLSI (Prentice Hall), 1990, pp. 174 - 232
	BB	Chew et al., "Impact of 0.25μm Dual Gate Oxide CMOS Process on the Flicker Noise Characteristics of Multi-Fingered MOSFETs for Wireless Applications", 2001 Int'l Symp. VLSI Tech., Systems , and Appl'ns, Procs. Tech. Paps., 18 - 20 Apr. 2001, pp. 220 - 223
	BC	Chew et al., "Impact of 0.25μm dual gate oxide thickness CMOS process on flicker noise performance of multi-fingered deep-submicron MOS devices", IEEE Procs.-Circuits Devices Systs., Dec. 2001, pp. 312 - 317
	BD	Cunningham, "CMOS Technology . . . Overcoming Yield Problems", Technology Assocs. and O.D. Trapp, 1987, pp. 9 - 22
	BE	Davari et al., "A High Performance 0.25 μm CMOS Technology", IEDM Tech. Dig., 11 - 14 Dec. 1988, pp. 56 - 59
	BF	El-Kareh, Fundamentals of Semiconductor Processing Technologies (Kluwer Acad. Pubs.), 1995, pp. 445 - 466
	BG	Faggin et al., "Silicon Gate Technology", Solid-State Electronics, vol. 13, 1970, pp. 1125 - 1144
	BH	Fujii et al., "A 45ns 16Mb DRAM with Triple-Well Structure", IEEE Int'l Solid-State Circs. Conf., Dig. Tech. Paps., 1989, pp. 248, 249, and 354
	BI	Fujii et al., "A 45-ns 16-Mbit DRAM with Triple-Well Structure", IEEE J. Solid-State Circs., Oct. 1989, pp. 1170 - 1175
	BJ	Gray et al., Analysis and Design of Analog Integrated Circuits (John Wiley & Sons), 1977, pp. 607 - 673
	BK	Grove, Physics and Technology of Semiconductor Devices (John Wiley & Sons), 1967, pp. 108 - 110 and 342 - 345
	BL	Hillenius et al., "Gate Material Work Function Considerations For 0.5 Micron CMOS", Procs. IEEE Int'l Conf. Computer Design: VLSI in Computers, 7 - 10 Oct. 1985, pp. 147 - 150
	BM	Hu et al., "Design and Fabrication of P-channel FET for 1-μm CMOS Technology," IEDM Tech. Dig., 11 - 15 Dec. 1982, pp. 710 - 713
	BN	Hung et al., "A 25.9-GHz Voltage-Controlled Oscillator in a CMOS Process", 2000 Symp. VLSI Circs., Dig. Tech Paps., 2000, pp. 100 and 101
	BO	Hung et al., "A Fully Integrated 5.35-GHz CMOS VCO and a Prescaler", 2000 IEEE Radio Freq. Integ. Circs. Symp., 2000, pp. 69 - 72
	BP	Hung et al., "A Packaged 1.1-GHz CMOS VCO with Phase Noise of -126 dBc/Hz at a 600-kHz Offset", IEEE J. Solid-State Circs., Jan. 2000, pp. 100 - 103
	BQ	Kimijima et al., "Improvement of 1/f noise by using VHP (Vertical High Pressure) oxynitride gate insulator for deep-submicron RF and analog CMOS", 1999 Symp. VLSI Tech., Dig. Tech Paps., 1999, pp. 119 and 120
	BR	King et al., "A Polycrystalline-$Si_{1-x}Ge_x$-Gate CMOS Technology", IEDM Tech. Dig., 9 - 12 Dec. 1990, pp. 253 - 256
	BS	Kooi et al., "Selective Oxidation of Silicon and its Device Applications", Semiconductor Silicon, 1973, pp. 860 - 879

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		OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)
	CA	Kooi, The Invention of LOCOS (Inst. Electrical and Electronics Engrs.), 1991, pp. 1 - 5
	CB	Lee et al., "Gate Oxide Thinning Effects at the Edge of Shallow Trench Isolation in the Dual Gate Oxide Process", 6th Int'l Conf. VLSI and CAD, 26 and 27 Oct. 1999, pp. 249 - 352
	CC	Lee et al., The Design of CMOS Radio-Frequency Integrated Circuits (Cambridge Univ. Press), 1998, pp. 252 - 255
	CD	Li et al., "A Comparison of CMOS and SiGe LNA's and Mixers for Wireless LAN Application", Procs. Custom Integ. Circs. Conf., 2001, pp. 531 - 534
	CE	Liu et al., "Multiple Gate Oxide Thickness for 2GHz System-on-A-Chip Technologies", IEDM Tech. Dig., 6 - 9 Dec. 1998, pp. 589 - 592
	CF	Meyer et al., "Integrable High Voltage CMOS: Devices, Process Application", IEDM Tech. Dig., 1 - 4 Dec. 1985, pp. 732 - 735
	CG	Mihaila et al., "Nonlinear Effects in the 1/f Noise of a 2D Electron Gas", Int'l J. Chaos Theory and Appl'ns, vol. 6, no. 3, 2001, pp. 47 - 55.
	CH	Mihaila, "Image of Phonon Spectrum in the 1/f Noise of Semiconductors", Procs. 1999 Int'l Semiconductor Conf., 5 - 9 Oct. 1999, pp. 117 - 120
	CI	Mihaila, "Low-frequency Noise in Nanomaterials and Nanodevices", Procs. 2001 Int'l Semiconductor Conf., 9 - 13 Oct. 2001, pp. 31 - 36
	CJ	Montree et al., "Comparison of buried and surface channel PMOS devices for low voltage 0.5 μm CMOS", 1993 Int'l Symp. VLSI Tech., Systems, and Appl'ns, Procs. Tech. Paps., 12 - 14 May 1993, pp. 11 - 14
	CK	Murthy et al., "Threshold-Voltage Anomaly in Sub-0.2μm DRAM Buried-Channel pFET Devices", 2001 Int'l Symp. VLSI Tech., Systems, and Appl'ns, Procs. Tech. Paps., 18 - 20 Apr. 2001, pp. 19 - 22
	CL	Muth, "Matrix Method for Latch-up Free Demonstration in a Triple-Well Bulk-Silicon Technology", IEEE Trans. Nuclear Sci., vol. 39, 1992, pp. 396 - 400
	CM	Nakahara et al., "Relief of hot carrier constraint on submicron CMOS devices by use of a buried channel structure", IEDM Tech. Dig., 1 - 4 Dec. 1985, pp. 238 - 241.
	CN	Nemirovsky et al., "1/f Noise in CMOS Transistors for Analog Applications", IEEE Trans Elec. Devs., May 2001, pp. 921 - 927
	CO	Ng, Complete Guide to Semiconductor Devices (McGraw-Hill), 1995, pp. 573 - 575
	CP	Nguyen et al, "A Comparison of Buried Channel and Surface Channel MOSFETs for VLSI", IEEE Trans. Elect. Devs., Oct. 1982, pp. 1663 and 1664.
	CQ	Nishida et al., "SoC CMOS Technology for NBTI/HCI Immune I/O and Analog Circuits Implementing Surface and Buried Channel Structures", IEDM Tech. Dig., 2 - 5 Dec. 2001, pp. 39.4.1 - 39.4.4
	CR	Nishiuchi et al., "A Normally-off Type Buried Channel MOSFET for VLSI Circuits", IEDM Tech. Dig., Dec. 1978, pp. 26 - 29
	CS	O et al., "1/f Noise of NMOS and PMOS Transistors and their Implications to Design of Voltage Controlled Oscillators", 2002 IEEE Radio Freq. Integ. Circs. Symp., 2002, pp. 59 - 62
	CT	O et al., "CMOS Components for 802.11b Wireless LAN Applications", 2002 IEEE Radio Freq. Integ. Circs. Symp., 2002, pp. 103 - 106

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		OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)
	DA	O et al., "Integration of Two Different Gate Oxide Thicknesses in a 0.6-μm Dual Voltage Mixed Signal CMOS Process", IEEE Trans. Elec. Devs., Jan. 1995, pp. 190 - 192
	DB	Ohguro et al., "A study of analog characteristics of CMOS with heavily nitrided NO oxynitrides", 2001 Symp. VLSI Tech., Dig. Tech. Paps., 2001, 2 pp.
	DC	Ohzone et al., "Silicon-Gate n-Well CMOS Process by Full Ion-Implantation Technology", IEEE Trans Elec. Devs., Sep. 1980, pp. 1789 - 1795
	DD	Park et al., "A Comparison of 1/f Noise of 0.25 μm-NMOS and PMOS Transistors from Deep-subthreshold to Strong Inversion", Int'l Conf. Noise in Physical Systems and 1/f Fluctuations, 2002, pp. 153 - 156
	DE	Park et al., "Body Bias Dependence of 1/f Noise in NMOS Transistors from Deep-Subthreshold to Strong Inversion", IEEE Trans Elec. Devs., May 2001, pp. 999 - 1001
	DF	Parrillo et al., "A Fine-Line CMOS Technology That Uses P^+ - Polysilicon/Silicide Gates For NMOS and PMOS Devices," IEDM Tech. Dig., Dec. 1984, pp. 418 - 422
	DG	Parrillo et al., "Twin-Tub CMOS - A Technology for VLSI Circuits", IEDM Tech. Dig., 8 - 10 Dec. 1980, pp. 752 - 755
	DH	Razavi, "CMOS Technology Characterization for Analog and RF Design", IEEE J. Solid-State Circs., Mar. 1999, pp. 268 - 276
	DI	Stolk et al., "CMOS Device Optimization for Mixed-Signal Technologies", IEDM Tech. Dig., 2 - 5 Dec. 2001, 4 pp.
	DJ	Sun et al., "The Junction MOS (JMOS) Transistor - A High Speed Transistor for VLSI", IEDM Tech. Dig., 8 - 10 Dec. 1980, pp. 791 - 794
	DK	Sze, VLSI Technology (McGraw-Hill), 1988, pp. 272 - 279 and 316 - 319
	DL	Taur et al., Fundamentals of VLSI Devices (Cambridge Univ. Press), 1998, pp. 58 - 90
	DM	Tsividis, Operation and Modeling of the MOS Transistor (McGraw-Hill), 1987, pp. 409 - 444
	DN	Vandamme et al., "1/f Noise in MOS Devices, Mobility or Number Fluctuations?", IEEE Trans. Elec. Devs., Nov. 1994, pp. 1936 - 1945
	DO	Vandamme, "Bulk and Surface 1/f Noise", IEEE Trans. Elec. Devs., May 1989, pp. 987 - 992
	DP	Wanlass et al., "Nanowatt Logic Using Field-Effect Metal-Oxide Semiconductor Triodes", ISSCC Dig. Tech. Paps., 1963, pp. 32 and 33
	DQ	Wong et al., "Doping of n+ and p+ Polysilicon in a Dual-gate CMOS Process", IEDM Tech. Dig., 11 - 14 Dec. 1988, pp. 238 - 241
	DR	Yeap et al., "A 100nm Copper Low-K Bulk CMOS Technology with Multi Vt and Multi Gate Oxide Integrated Transistors for Low Standby Power, High Performance and RF/Analog System on Chip Applications", 2002 Symp. VLSI Tech., Dig. Tech. Paps., 2002, pp. 16 and 17
	DS	Yeap et al., "A 180nm Copper/Low-k CMOS Technology with Dual Gate Oxide Optimized for Low Power and Low Cost Consumer Wireless Applications", 2000 Symp. VLSI Tech., Dig. Tech. Paps., 2000, pp. 150 and 151
	DT	"Piranha/HF clean: View", MEMS Exchange, www.mems-exchange.org/catalog/P2568, undated, 3 pp.

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